REMARKS/ARGUMENTS

Claims 1-30 are pending in the present application.

This Amendment is in response to the final Office Action mailed February 18, 2005. In the final Office Action, the Examiner rejected claims 1-2, 10, 11-12, 20, 21-22 and 30 under 35 U.S.C. §103(a). In addition, the Examiner indicated allowable subject matter for claims 3-9, 13-19, and 23-29 if they are rewritten in independent form including all of the limitations of the base claim and any intervening claims. Applicants have amended claims 1-3, 6-9, 11-19, 21-23, and 26-29. Reconsideration in light of the amendments and remarks made herein is respectfully requested.

Rejection Under 35 U.S.C. § 103

1. In the final Office Action, the Examiner rejected claims 1-2, 10, 11-12, 20, 21-22 and 30 under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 5,381,533 issued to Peleg et al. ("Peleg") in view of U.S. Patent No. 6,397,296 issued to Werner ("Werner").

Applicants respectfully traverse the rejection and contend that the Examiner has not met the burden of establishing a prima facie case of obviousness. To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. *MPEP §2143, p. 2100-129 (8th Ed., Rev. 2, May 2004).* Applicants respectfully contend that there is no suggestion or motivation to combine their teachings, and thus no *prima facie* case of obviousness has been established.

Applicants reiterated the arguments presented in the previous response.

Peleg discloses a dynamic flow instruction cache memory organized around trace segments independent of virtual address line. A computer includes a central processing unit, a cache memory, and a line buffer (Peleg, col. 5, lines 18, 20-21, 44-45, 63-64; Figure 1, elements, 20, 21, 22, and 23). All cache memory inputs are from the line buffer. When the instruction in a

basic block are not found in the cache memory, they are obtained from the main memory and executed (Peleg, col. 8, lines 59-65, col. 9, lines 23-27).

Werner discloses a two-level instruction cache for embedded processors. A cache system includes an L1 cache, an L0 cache, and an assist cache. An assist filter is used with the assist cache (Werner, col. 3, lines 62-65). The assist cache has a victim cache and a prefetch cache. The victim cache includes a first set of cache lines for storing instructions that were displaced from the L0 cache (Werner, col. 4, lines 13-16). The assist filter includes a victim filter and a prefetch filter. The victim filter has a victim memory for storing a set of addresses or tags. The victim cache is responsive to the victim filter (Werner, col. 4, lines 13-22). The victim filter stores the most frequently accessed cache lines in the victim cache (Werner, col. 8, line 67 to col. 9, lines 1).

Peleg and Werner, taken alone or in any combination, do not disclose, suggest, or render obvious (1) managing transfer of a trace, (2) a first cache to evict the trace based on a replacement mechanism, and (3) a second cache to receive the evicted trace based on a number of accesses to the trace as discussed above. There is no motivation to combine Peleg and Werner because none of them addresses the problem of trace cache filtering. There is no teaching or suggestion that a second cache to receive the evicted trace based on number of accesses is present. Peleg, read as a whole, does not suggest the desirability of filtering trace cache.

Peleg merely discloses obtaining instructions form the main memory if they are not found in the cache. Peleg does not disclose a cache management logistics to control a transfer of a trace. Element 20 is a computer which includes the execution unit and the cache, not a cache manager. In the Final Office Action dated February 17, 2005, the Examiner states that "it is inherent to have a controller or management logistics to control a cache in a computer system including the cache" (Final Office Action, Page 4). Applicants respectfully disagree.

The Examiner apparently relied on the "official notice" to arrive at such a conclusion because the Examiner did not provide any prior art reference teaching or suggesting the above feature. Applicants contend that such an official notice is inappropriate.

Official notice unsupported by documenting evidence should only be taken by the Examiner where the facts asserted to be well-known, or to be common knowledge in the art are capable of instant and unquestionable demonstration as being well known. In re Ahlert, 424 F.2d

1088, 1091, 165 USPQ 418, 420 (CCPA 1970); MPEP 2144.03A. It would not be appropriate for the Examiner to take official notice of facts without citing a prior art references. MPEP 2144.03A. Furthermore, if official notice is taken of a fact, unsupported by documentary evidence, the technical line of reasoning underlying a decision to take such notice must be clear and unmistakable. MPEP 2144.03B.

Here, neither Peleg nor Werner discloses or suggests the use of a manager to manage transfer of a trace. The Examiner did not provide a technical line of reasoning which must be clear and unmistakable. The Examiner merely states that "it would have been readily appreciated by one of ordinary skill in the art that a computer system having caches includes management logistics or a cache controller to control cache operation, such as transfer of data to and from the caches." (Final Office Action, Page 4). However, "control cache operation" is not the same as "managing a transfer of a trace". Furthermore, "transfer of data" is not the same as "transfer of a trace". A trace is defined as a sequence of basic blocks that have been executed by the program. Therefore, the Examiner's reasoning is unclear and not unmistakable.

The Examiner further states "Peleg discloses . . . to evict the trace based on a replacement mechanism", noting that replacement algorithm and cache miss reads on this limitation, since a line is needed to evict to free up a space for a new entry (Final Office Action, page 4, last paragraph, and Page 5, lines 1-2). Applicants respectfully disagree. First, a cache miss does not necessarily result in evicting a trace. Peleg merely discloses obtaining the instructions not found in cache from the memory when there is a cache miss. Peleg does not disclose or suggest evicting a trace when obtaining the instructions from the memory. Second, Peleg does not suggest a second cache to receive the evicted trace based on number of accesses to the trace.

The Examiner further states that Werner discloses eviction mechanism (Final Office Action, Page 5, second full paragraph), citing Col. 8, line 65 through col. 9, line 8 ("the victim cache accepts every displaced cache line.") Applicants respectfully disagree.

Werner merely discloses a victim filter storing the most frequently accessed cache lines in the victim cache, not to receive the evicted trace based on number of accesses. The most frequently accessed cache lines are not evicted trace. In fact, Werner essentially teaches away from the invention because while Werner teaches storing, the claims recite evicting. "Storing" and "evicting" are two opposite operations. Werner merely discloses "the victim cache accepts

every displaced cache line" (Werner, Col. 8, lines 65-66, emphasis added). A "displaced cache line" is not the same as an "evicted trace". In addition, Werner does not teach or suggest "based on a first number of accesses to the trace" because accepting every displaced cache line means that accepting all displaced cache lines without condition.

Claims 1-3, 6-9, 11-19, 21-23, and 26-29 have been amended to clarify the claim language and to correct minor informalities.

Therefore, Applicants believe that independent claims 1, 11, 21 and their respective dependent claims are distinguishable over the cited prior art references. Accordingly, Applicants respectfully request the rejections under 35 U.S.C. §103(a) be withdrawn.

Allowable Subject Matter

1. In the final Office Action, the Examiner indicated allowable subject matter for claims 3-9, 13-19, and 23-29 if they are rewritten in independent form including all of the limitations of the base claim and any intervening claims. In light of the above amendments and remarks, Applicants respectfully request the objections be withdrawn.

Conclusion

Applicant respectfully requests that a timely Notice of Allowance be issued in this case.

Respectfully submitted,

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